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This invention relates generally to semiconductor memory devices and, more particularly, to bitline sense amplifier circuits for dynamic semiconductor memory devices. As is known in the art, a dynamic semiconductor memory device (referred to as a DRAM or memory herein) includes an array of memory cells that are arranged in rows and columns. Each memory cell includes a capacitor which stores information (e.g., a logic state) therein. Typically, each memory cell is electrically coupled to a wordline (WL) and a bitline. Each bitline is coupled to a sense amplifier that provides differential sensing of the stored information. More particularly, a DRAM typically includes a matrix of memory cells, arranged in rows and columns, that is accessed by using digit lines (DL) that extend in parallel to each other (each DL having a DL and a bar DL), and wordlines (WLs) that extend perpendicular to each other (each WL having a WL and a bar WL). Typically, all of the DLs are electrically coupled to one of the bar WLs, and the memory cells in a row are connected to a single wordline. As a result, a memory cell in a given row that is accessed by the single wordline can be accessed by activating its corresponding bar WL. Once activated, a bar WL applies a voltage to its corresponding wordlines to activate memory cells along the corresponding row. Consequently, the memory cells along a row can be accessed by activating its corresponding bar WL and applying a voltage to its corresponding wordlines. Unfortunately, due to the physical arrangement of the memory cells within the array, the DLs and the bar DLs that are electrically coupled to the same bar WL may include capacitive coupling (i.e., crosstalk). For example, if a memory cell that is 2d92ce491b